

## TimerBlox: Monostable Pulse Generator (One Shot)

### FEATURES

- **Pulse Width Range: 1μs to 33.6 Seconds**
- Configured with 1 to 3 Resistors
- Pulse Width Max Error:
  - <2.3% for Pulse Width > 512μs
  - <3.4% for Pulse Width of 8μs to 512μs
  - <4.9% for Pulse Width of 1μs to 8μs
- Four LTC6993 Options Available:
  - Rising-Edge or Falling-Edge Trigger
  - Retriggerable or Non-Retriggerable
- Configurable for Positive or Negative Output Pulse
- Fast Recovery Time
- 2.25V to 5.5V Single Supply Operation
- 70μA Supply Current at 10μs Pulse Width
- 500μs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –40°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN

### APPLICATIONS

- Watchdog Timer
- Frequency Discriminators
- Missing Pulse Detection
- Envelope Detection
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

### DESCRIPTION

The LTC®6993 is a monostable multivibrator (also known as a “one-shot” pulse generator) with a programmable pulse width of 1μs to 33.6 seconds. The LTC6993 is part of the TimerBlox™ family of versatile silicon timing devices.

A single resistor,  $R_{SET}$ , programs the LTC6993's internal master oscillator frequency. The output pulse width is determined by this master oscillator and an internal clock divider,  $N_{DIV}$ , programmable to eight settings from 1 to  $2^{21}$ .

$$t_{OUT} = \frac{N_{DIV} \cdot R_{SET}}{50k\Omega} \cdot 1\mu s, N_{DIV} = 1, 8, 64, \dots, 2^{21}$$

The output pulse is initiated by a transition on the trigger input (TRIG). Each part can be configured to generate positive or negative output pulses. The LTC6993 is available in four versions to provide different trigger signal polarity and retrigger capability.

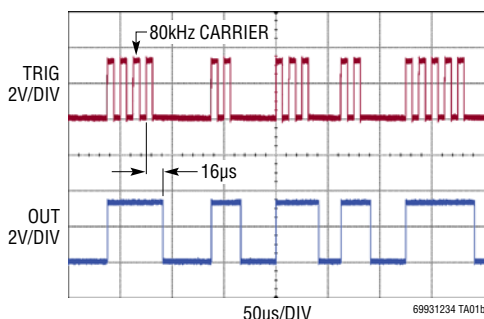
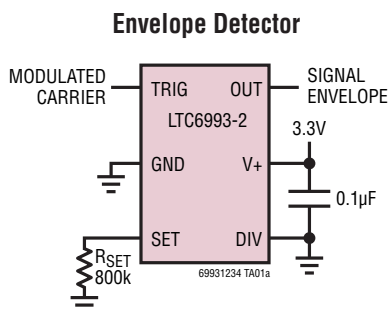
DEVICE	INPUT POLARITY	RETRIGGER
LTC6993-1	Rising-Edge	No
LTC6993-2	Rising-Edge	Yes
LTC6993-3	Falling-Edge	No
LTC6993-4	Falling-Edge	Yes

The LTC6993 also offers the ability to dynamically adjust the width of the output pulse via a separate control voltage.

The LTC6993 is available in the 6-lead SOT-23 (ThinSOT) and 6-lead 2mm × 3mm DFN packages.

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### TYPICAL APPLICATION



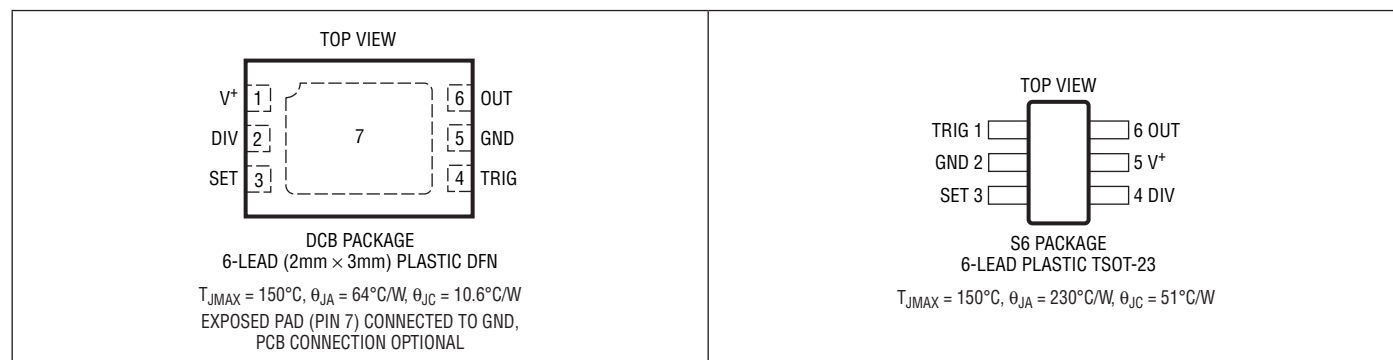
# LTC6993-1/LTC6993-2 LTC6993-3/LTC6993-4

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+) to GND .....6V  
Maximum Voltage  
on Any Pin ..... (GND – 0.3V) ≤ V<sub>PIN</sub> ≤ (V<sup>+</sup> + 0.3V)  
Operating Temperature Range (Note 2)  
LTC6993C .....–40°C to 85°C  
LTC6993I .....–40°C to 85°C  
LTC6993H.....–40°C to 125°C

Specified Temperature Range (Note 3)  
LTC6993C ..... 0°C to 70°C  
LTC6993I .....–40°C to 85°C  
LTC6993H.....–40°C to 125°C  
Junction Temperature ..... 150°C  
Storage Temperature Range .....–65°C to 150°C  
Lead Temperature (Soldering, 10 sec)  
S6 Package.....300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6993CDCB-1#PBF	LTC6993CDCB-1#TRPBF	LDXH	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6993IDCB-1#PBF	LTC6993IDCB-1#TRPBF	LDXH	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6993HDCB-1#PBF	LTC6993HDCB-1#TRPBF	LDXH	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6993CDCB-2#PBF	LTC6993CDCB-2#TRPBF	LDXK	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6993IDCB-2#PBF	LTC6993IDCB-2#TRPBF	LDXK	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6993HDCB-2#PBF	LTC6993HDCB-2#TRPBF	LDXK	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6993CDCB-3#PBF	LTC6993CDCB-3#TRPBF	LFMJ	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6993IDCB-3#PBF	LTC6993IDCB-3#TRPBF	LFMJ	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6993HDCB-3#PBF	LTC6993HDCB-3#TRPBF	LFMJ	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6993CDCB-4#PBF	LTC6993CDCB-4#TRPBF	LFMM	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6993IDCB-4#PBF	LTC6993IDCB-4#TRPBF	LFMM	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6993HDCB-4#PBF	LTC6993HDCB-4#TRPBF	LFMM	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6993CS6-1#PBF	LTC6993CS6-1#TRPBF	LTDXG	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6993IS6-1#PBF	LTC6993IS6-1#TRPBF	LTDXG	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6993HS6-1#PBF	LTC6993HS6-1#TRPBF	LTDXG	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6993CS6-2#PBF	LTC6993CS6-2#TRPBF	LTDXJ	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6993IS6-2#PBF	LTC6993IS6-2#TRPBF	LTDXJ	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6993HS6-2#PBF	LTC6993HS6-2#TRPBF	LTDXJ	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6993CS6-3#PBF	LTC6993CS6-3#TRPBF	LTFMH	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6993IS6-3#PBF	LTC6993IS6-3#TRPBF	LTFMH	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6993HS6-3#PBF	LTC6993HS6-3#TRPBF	LTFMH	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6993CS6-4#PBF	LTC6993CS6-4#TRPBF	LTFMK	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6993IS6-4#PBF	LTC6993IS6-4#TRPBF	LTFMK	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6993HS6-4#PBF	LTC6993HS6-4#TRPBF	LTFMK	6-Lead Plastic TSOT-23	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $\text{TRIG} = 0\text{V}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $2^{21}$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{OUT}}$	Output Pulse Width		1 $\mu$		33.55	sec
$\Delta t_{\text{OUT}}$	Pulse Width Accuracy (Note 4)	$N_{\text{DIV}} \geq 512$	●	$\pm 1.7$	$\pm 2.3$ $\pm 3.0$	% %
		$8 \leq N_{\text{DIV}} \leq 64$	●	$\pm 2.4$	$\pm 3.4$ $\pm 4.4$	% %
		$N_{\text{DIV}} = 1$ (LTC6993-1 or LTC6993-2)	●	$\pm 3.6$	$\pm 4.9$ $\pm 6.0$	% %
		$N_{\text{DIV}} = 1$ (LTC6993-3 or LTC6993-4)	●	$\pm 4.0$	$\pm 5.3$ $\pm 6.4$	% %
$\Delta t_{\text{OUT}}/\Delta T$	Pulse Width Drift Over Temperature	$N_{\text{DIV}} \geq 512$	●	$\pm 0.006$		%/ $^\circ\text{C}$
		$N_{\text{DIV}} \leq 64$	●	$\pm 0.008$		%/ $^\circ\text{C}$
	Pulse Width Change With Supply	$N_{\text{DIV}} \geq 512$	●	$-0.6$	$-0.2$	%
			●	$-0.4$	$-0.1$	%
		$8 \leq N_{\text{DIV}} \leq 64$	●	$-0.9$	$-0.2$	%
			●	$-0.7$	$-0.2$	%
			●	$-1.1$	$-0.1$	%
	Pulse Width Jitter (Note 10)	$N_{\text{DIV}} = 1$		0.85		%p-p
				0.45		%p-p
		$N_{\text{DIV}} = 8$		0.20		%p-p
		$N_{\text{DIV}} = 64$		0.05		%p-p
		$N_{\text{DIV}} = 512$		0.20		%p-p
$t_s$	Pulse Width Change Settling Time (Note 9)	$N_{\text{DIV}} = 4096$		0.03		%p-p
		$t_{\text{MASTER}} = t_{\text{OUT}}/N_{\text{DIV}}$		$6 \cdot t_{\text{MASTER}}$		$\mu\text{s}$

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# LTC6993-1/LTC6993-2

# LTC6993-3/LTC6993-4

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $\text{TRIG} = 0\text{V}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $2^{21}$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V <sup>+</sup>	Operating Supply Voltage Range		●	2.25		5.5	V
	Power-On Reset Voltage		●			1.95	V
I <sub>S(IDLE)</sub>	Supply Current (Idle)	R <sub>L</sub> = ∞, R <sub>SET</sub> = 50k, N <sub>DIV</sub> ≤ 64 V <sup>+</sup> = 5.5V V <sup>+</sup> = 2.25V	● ●		165 125	200 160	μA μA
		R <sub>L</sub> = ∞, R <sub>SET</sub> = 50k, N <sub>DIV</sub> ≥ 512 V <sup>+</sup> = 5.5V V <sup>+</sup> = 2.25V	● ●		135 105	175 140	μA μA
		R <sub>L</sub> = ∞, R <sub>SET</sub> = 800k, N <sub>DIV</sub> ≤ 64 V <sup>+</sup> = 5.5V V <sup>+</sup> = 2.25V	● ●		70 60	110 95	μA μA
		R <sub>L</sub> = ∞, R <sub>SET</sub> = 800k, N <sub>DIV</sub> ≥ 512 V <sup>+</sup> = 5.5V V <sup>+</sup> = 2.25V	● ●		65 55	100 90	μA μA
Analog Inputs							
V <sub>SET</sub>	Voltage at SET Pin		●	0.97	1.00	1.03	V
ΔV <sub>SET</sub> /ΔT	V <sub>SET</sub> Drift Over Temperature		●		±75		μV/°C
R <sub>SET</sub>	Frequency-Setting Resistor		●	50		800	kΩ
V <sub>DIV</sub>	DIV Pin Voltage		●	0		V <sup>+</sup>	V
ΔV <sub>DIV</sub> /ΔV <sup>+</sup>	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V <sub>DIV</sub> /V <sup>+</sup> = (DIVCODE + 0.5)/16	●			±1.5	%
	DIV Pin Input Current		●			±10	nA
Digital I/O							
	TRIG Pin Input Capacitance				2.5		pF
	TRIG Pin Input Current	TRIG = 0V to V <sup>+</sup>				±10	nA
V <sub>IH</sub>	High Level TRIG Pin Input Voltage	(Note 6)	●	0.7 • V <sup>+</sup>			V
V <sub>IL</sub>	Low Level TRIG Pin Input Voltage	(Note 6)	●			0.3 • V <sup>+</sup>	V
I <sub>OUT(MAX)</sub>	Output Current	V <sup>+</sup> = 2.7V to 5.5V			±20		mA
V <sub>OH</sub>	High Level Output Voltage (Note 7)	V <sup>+</sup> = 5.5V I <sub>OUT</sub> = −1mA I <sub>OUT</sub> = −16mA	● ●	5.45 4.84	5.48 5.15		V V
		V <sup>+</sup> = 5.5V I <sub>OUT</sub> = −1mA I <sub>OUT</sub> = −16mA	● ●	3.24 2.75	3.27 2.99		V V
		V <sup>+</sup> = 2.25V I <sub>OUT</sub> = −1mA I <sub>OUT</sub> = −8mA	● ●	2.17 1.58	2.21 1.88		V V
V <sub>OL</sub>	Low Level Output Voltage (Note 7)	V <sup>+</sup> = 5.5V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 16mA	● ●		0.02 0.26	0.04 0.54	V V
		V <sup>+</sup> = 3.3V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 10mA	● ●		0.03 0.22	0.05 0.46	V V
		V <sup>+</sup> = 2.25V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 8mA	● ●		0.03 0.26	0.07 0.54	V V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $\text{TRIG} = 0\text{V}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $2^{21}$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = \infty$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{PD}}$	Trigger Propagation Delay	$V^+ = 5.5\text{V}$ $V^+ = 3.3\text{V}$ $V^+ = 2.25\text{V}$		11 17 28		ns ns ns
$t_{\text{WIDTH}}$	Minimum Recognized TRIG Pulse Width	$V^+ = 3.3\text{V}$		5		ns
$t_{\text{ARM}}$	Recovery Time (LTC6993-1/LTC6993-3)			–4		ns
$t_{\text{RETRIG}}$	Time Between Trigger Signals (LTC6993-2/LTC6993-4)	$N_{\text{DIV}} = 1$ $V^+ = 3.3\text{V}$ $N_{\text{DIV}} > 1$ $V^+ = 3.3\text{V}$		10 50		ns ns
$t_r$	Output Rise Time (Note 8)	$V^+ = 5.5\text{V}$ $V^+ = 3.3\text{V}$ $V^+ = 2.25\text{V}$		1.1 1.7 2.7		ns ns ns
$t_f$	Output Fall Time (Note 8)	$V^+ = 5.5\text{V}$ $V^+ = 3.3\text{V}$ $V^+ = 2.25\text{V}$		1.0 1.6 2.4		ns ns ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6993C is guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**Note 3:** The LTC6993C is guaranteed to meet specified performance from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The LTC6993C is designed, characterized and expected to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  but it is not tested or QA sampled at these temperatures. The LTC6993I is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6993H is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 4:** Frequency accuracy is defined as the deviation from the  $f_{\text{OUT}}$  equation, assuming  $R_{\text{SET}}$  is used to program the frequency.

**Note 5:** See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

**Note 6:** The TRIG pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to  $V^+$ . Typical values can be estimated at any supply voltage using:

$$V_{\text{TRIG(RISING)}} \approx 0.55 \cdot V^+ + 185\text{mV and}$$

$$V_{\text{TRIG(FALLING)}} \approx 0.48 \cdot V^+ - 155\text{mV}$$

**Note 7:** To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with  $5\text{pF}$  output load. These specifications are based on characterization.

**Note 9:** Settling time is the amount of time required for the output to settle within  $\pm 1\%$  of the final pulse width after a  $0.5\times$  or  $2\times$  change in  $I_{\text{SET}}$ .

**Note 10:** Jitter is the ratio of the deviation of the output pulse width to the mean of the pulse width. This specification is based on characterization and is not 100% tested.

**TYPICAL PERFORMANCE CHARACTERISTICS**

$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^{\circ}C$  unless otherwise noted.

$t_{OUT}$  Error vs Temperature  
( $N_{DIV} = 1$ )

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( $N_{DIV} = 1$ )

$t_{OUT}$  Error vs Temperature  
( $8 \leq N_{DIV} \leq 64$ )

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$t_{OUT}$  Error vs Temperature  
( $N_{DIV} \geq 512$ )

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$t_{OUT}$  Error vs Temperature  
( $N_{DIV} \geq 512$ )

## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

$t_{OUT}$  Error vs DIVCODE

$t_{OUT}$  Error vs DIVCODE

$t_{OUT}$  Error vs DIVCODE

$t_{OUT}$  Error vs  $R_{SET}$  ( $N_{DIV} = 1$ )

$t_{OUT}$  Error vs  $R_{SET}$  ( $8 \leq N_{DIV} \leq 64$ )

$t_{OUT}$  Error vs  $R_{SET}$  ( $N_{DIV} \geq 512$ )

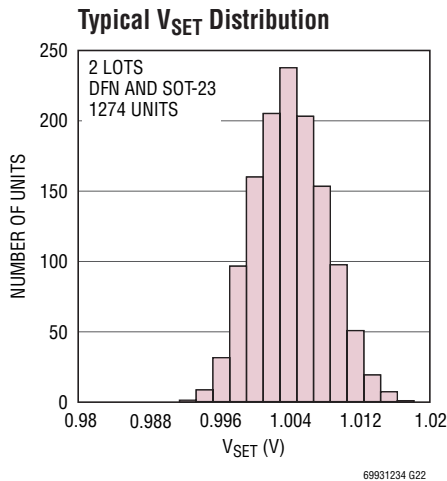
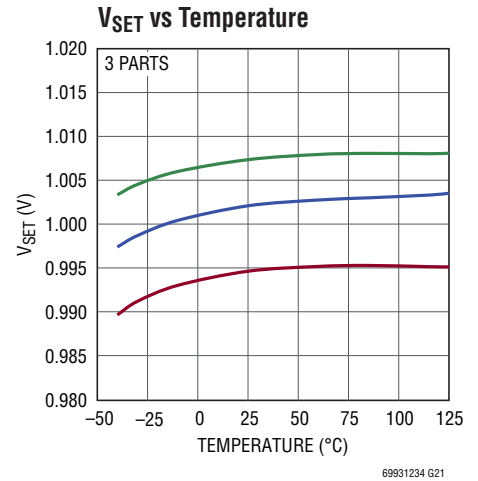
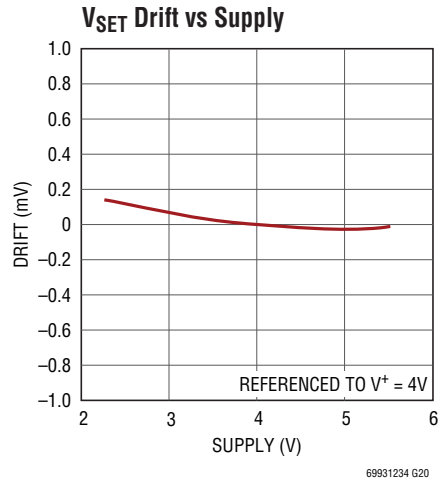
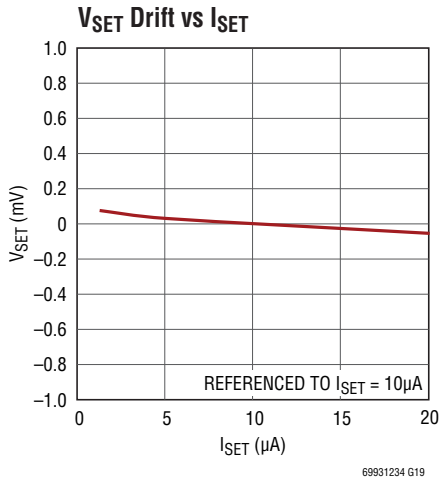
$t_{OUT}$  Drift vs Supply Voltage  
( $N_{DIV} = 1$ )

$t_{OUT}$  Drift vs Supply Voltage  
( $8 \leq N_{DIV} \leq 64$ )

$t_{OUT}$  Drift vs Supply Voltage  
( $N_{DIV} \geq 512$ )

## TYPICAL PERFORMANCE CHARACTERISTICS

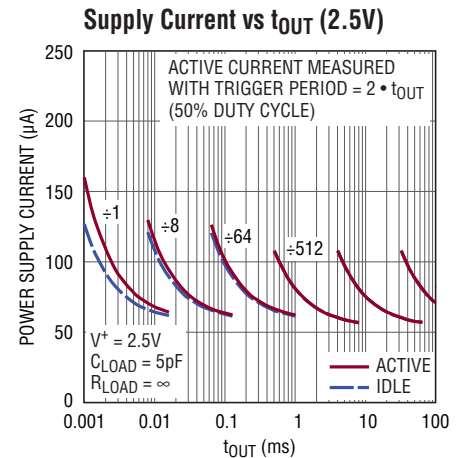
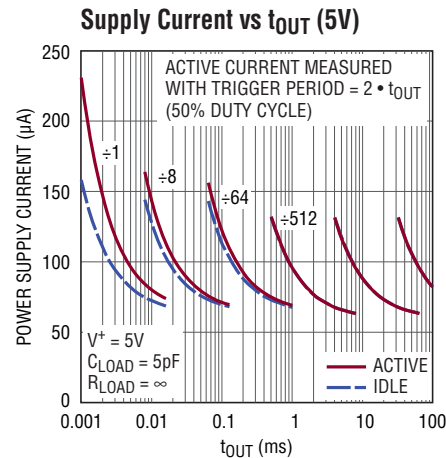
$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.



### Supply Current vs Supply Voltage

### Supply Current vs Temperature

### Supply Current vs TRIG Pin Voltage

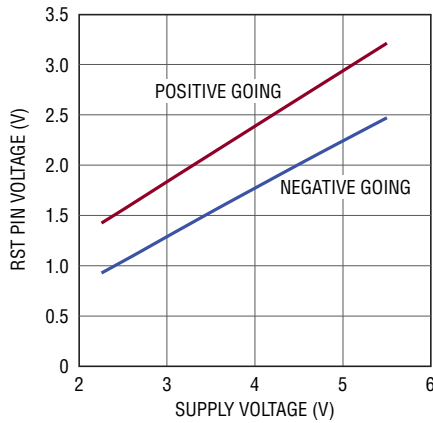




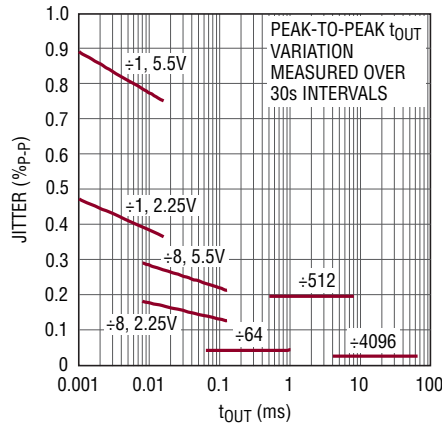
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$  and  $T_A = 25^\circ C$  unless otherwise noted.

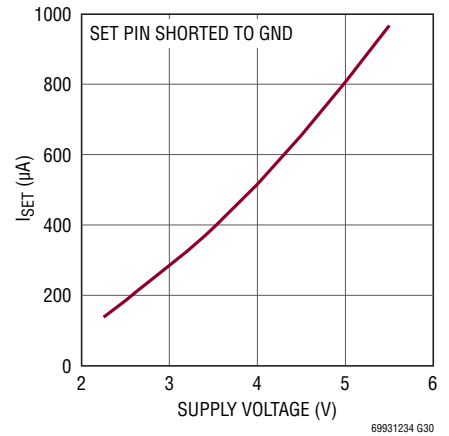
**TRIG Threshold Voltage vs Supply Voltage**



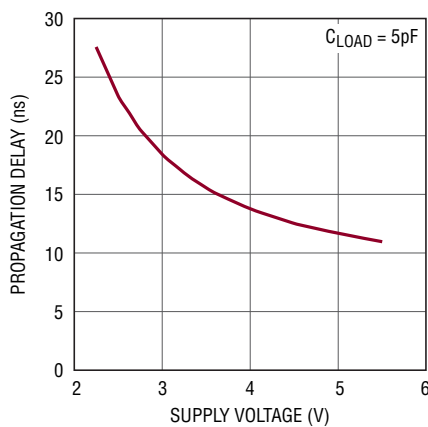
**Peak-to-Peak Jitter vs  $t_{OUT}$**



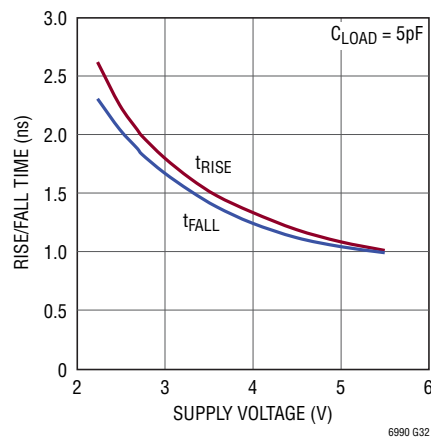
**Typical  $I_{SET}$  Current Limit vs  $V^+$**



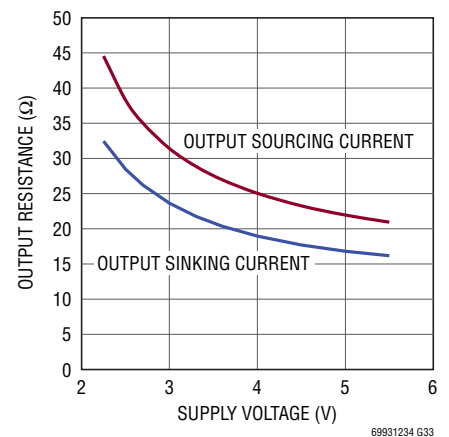
**Trigger Propagation Delay ( $t_{PD}$ ) vs Supply Voltage**



**Rise and Fall Time vs Supply Voltage**



**Output Resistance vs Supply Voltage**



## PIN FUNCTIONS (DCB/S6)

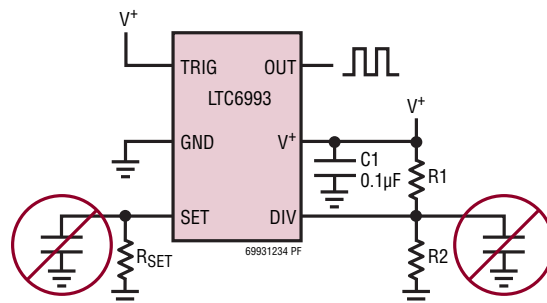
**V<sup>+</sup> (Pin 1/Pin 5):** Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1μF capacitor.

**DIV (Pin 2/Pin 4):** Programmable Divider and Polarity Input. The DIV pin voltage ( $V_{DIV}$ ) is internally converted into a 4-bit result (DIVCODE).  $V_{DIV}$  may be generated by a resistor divider between V<sup>+</sup> and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that  $V_{DIV}$  settles quickly. The MSB of DIVCODE (POL) determines the polarity of the OUT pins. When POL = 0 the output produces a positive pulse. When POL = 1 the output produces a negative pulse.

**SET (Pin 3/Pin 3):** Pulse Width Setting Input. The voltage on the SET pin ( $V_{SET}$ ) is regulated to 1V above GND. The amount of current sourced from the SET pin ( $I_{SET}$ ) programs the master oscillator frequency. The  $I_{SET}$  current range is 1.25μA to 20μA. The output pulse will continue indefinitely if  $I_{SET}$  drops below approximately 500nA, and will terminate when  $I_{SET}$  increases again. A resistor connected between SET and GND is the most accurate way to set the pulse width. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less

than 100pF maintains the stability of the feedback circuit regulating the  $V_{SET}$  voltage.



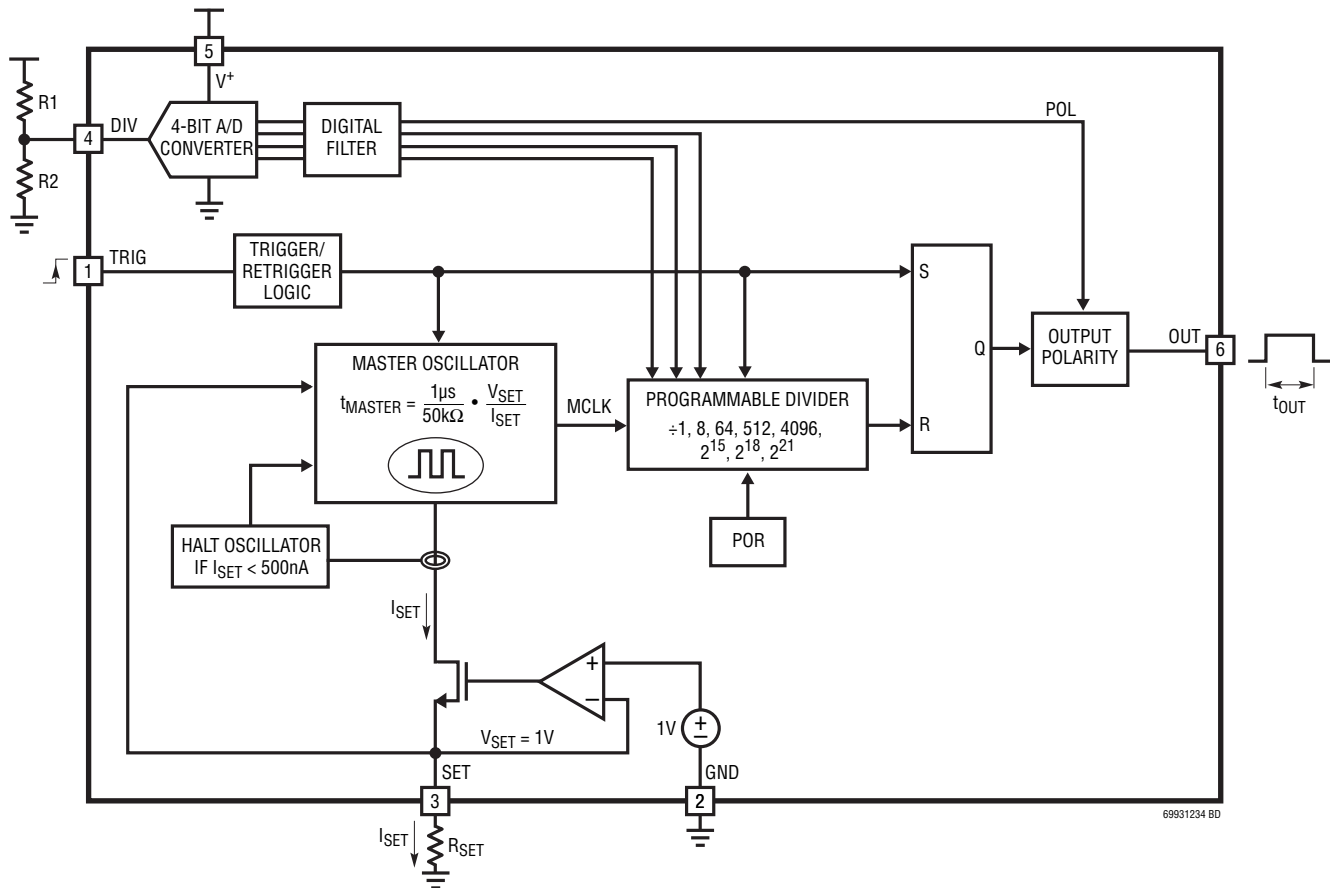
**TRIG (Pin 4/Pin 1):** Trigger Input. Depending on the version, a rising or falling edge on TRIG will initiate the output pulse. LTC6993-1 and LTC6993-2 are rising-edge sensitive. LTC6993-3 and LTC6993-4 are falling-edge sensitive.

The LTC6993-2 and LTC6993-4 are retriggerable, allowing the pulse width to be extended by additional trigger signals that occur while the output is active. The LTC6993-1/LTC6993-3 will ignore additional trigger inputs until the output pulse has terminated.

**GND (Pin 5/Pin 2):** Ground. Tie to a low inductance ground plane for best performance.

**OUT (Pin 6/Pin 6):** Output. The OUT pin swings from GND to V<sup>+</sup> with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.

## BLOCK DIAGRAM (S6 package pin numbers shown)



## OPERATION

The LTC6993 is built around a master oscillator with a 1μs minimum period. The oscillator is controlled by the SET pin current ( $I_{SET}$ ) and voltage ( $V_{SET}$ ), with a 1μs/50kΩ conversion factor that is accurate to ±1.7% under typical conditions.

$$t_{MASTER} = \frac{1\mu s}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}}$$

A feedback loop maintains  $V_{SET}$  at 1V ±30mV, leaving  $I_{SET}$  as the primary means of controlling the pulse width. The simplest way to generate  $I_{SET}$  is to connect a resistor ( $R_{SET}$ ) between SET and GND, such that  $I_{SET} = V_{SET}/R_{SET}$ . The master oscillator equation reduces to:

$$t_{MASTER} = 1\mu s \cdot \frac{R_{SET}}{50k\Omega}$$

From this equation, it is clear that  $V_{SET}$  drift will not affect the pulse width when using a single program resistor ( $R_{SET}$ ). Error sources are limited to  $R_{SET}$  tolerance and the inherent pulse width accuracy  $\Delta t_{OUT}$  of the LTC6993.

$R_{SET}$  may range from 50k to 800k (equivalent to  $I_{SET}$  between 1.25μA and 20μA).

A trigger signal (rising or falling edge on TRIG pin) latches the output to the active state, beginning the output pulse. At the same time, the master oscillator is enabled to time the duration of the output pulse. When the desired pulse width is reached, the master oscillator resets the output latch.

The LTC6993 also includes a programmable frequency divider which can further divide the frequency by 1, 8, 64, 512, 4096,  $2^{15}$ ,  $2^{18}$  or  $2^{21}$ . This extends the pulse width duration by those same factors. The divider ratio  $N_{DIV}$  is set by a resistor divider attached to the DIV pin.

$$t_{OUT} = \frac{N_{DIV}}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}} \cdot 1\mu s$$

With  $R_{SET}$  in place of  $V_{SET}/I_{SET}$  the equation reduces to:

$$t_{OUT} = \frac{N_{DIV} \cdot R_{SET}}{50k\Omega} \cdot 1\mu s$$

## DIVCODE

The DIV pin connects to an internal,  $V^+$  referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6993:

1. DIVCODE determines the frequency divider setting,  $N_{DIV}$ .
2. DIVCODE determines the polarity of OUT pin, via the POL bit.

$V_{DIV}$  may be generated by a resistor divider between  $V^+$  and GND as shown in Figure 1.

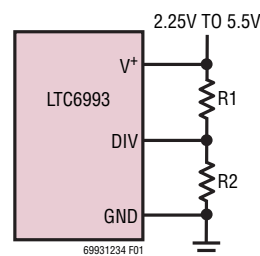


Figure 1. Simple Technique for Setting DIVCODE

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding  $N_{DIV}$  and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The  $V_{DIV}/V^+$  ratio is accurate to ±1.5% (including resistor tolerances and temperature effects).
2. The driving impedance ( $R1||R2$ ) does not exceed 500kΩ.

If the voltage is generated by other means (i.e., the output of a DAC) it must track the  $V^+$  supply voltage. The last column in Table 1 shows the ideal ratio of  $V_{DIV}$  to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4,  $V_{DIV} = 0.281 \cdot 3.3V = 928mV \pm 50mV$ .

Figure 2 illustrates the information in Table 1, showing that  $N_{DIV}$  is symmetric around the DIVCODE midpoint.

## OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N <sub>DIV</sub>	Recommended t <sub>OUT</sub>	R1 (k)	R2 (k)	V <sub>DIV</sub> /V <sup>+</sup>
0	0	1	1μs to 16μs	Open	Short	≤ 0.03125 ±0.015
1	0	8	8μs to 128μs	976	102	0.09375 ±0.015
2	0	64	64μs to 1.024ms	976	182	0.15625 ±0.015
3	0	512	512μs to 8.192ms	1000	280	0.21875 ±0.015
4	0	4,096	4.096ms to 65.54ms	1000	392	0.28125 ±0.015
5	0	32,768	32.77ms to 524.3ms	1000	523	0.34375 ±0.015
6	0	262,144	262.1ms to 4.194ms	1000	681	0.40625 ±0.015
7	0	2,097,152	2.097sec to 33.55sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2.097sec to 33.55sec	887	1000	0.53125 ±0.015
9	1	262,144	262.1ms to 4.194ms	681	1000	0.59375 ±0.015
10	1	32,768	32.77ms to 524.3ms	523	1000	0.65625 ±0.015
11	1	4,096	4.096ms to 65.54ms	392	1000	0.71875 ±0.015
12	1	512	512μs to 8.192ms	280	1000	0.78125 ±0.015
13	1	64	64μs to 1.024ms	182	976	0.84375 ±0.015
14	1	8	8μs to 128μs	102	976	0.90625 ±0.015
15	1	1	1μs to 16μs	Short	Open	≥ 0.96875 ±0.015

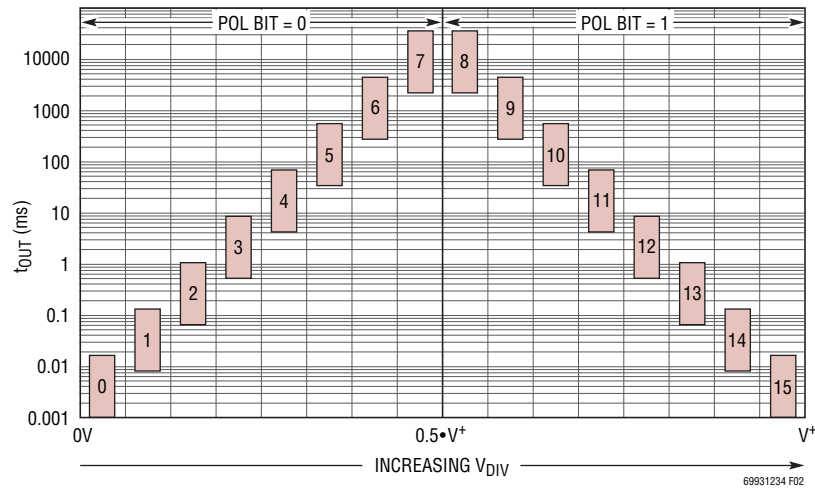


Figure 2. Pulse Width Range and POL Bit vs DIVCODE

OPERATION

Monostable Multivibrator (One Shot)

The LTC6993 is a monostable multivibrator. A trigger signal on the TRIG input will force the output to the active (unstable) state for a programmable duration. This type of circuit is commonly referred to as a one-shot pulse generator.

Figures 3 details the basic operation. A rising edge on the TRIG pin initiates the output pulse. The pulse width ( $t_{OUT}$ ) is determined by the  $N_{DIV}$  setting and by the resistor ( $R_{SET}$ ) connected to the SET pin. Subsequent rising edges on TRIG have no affect until the completion of the one shot and for a short rearming time ( $t_{ARM}$ ) thereafter. To ensure proper operation, positive and negative TRIG pulses should be at least  $t_{WIDTH}$  wide.

The LTC6993-2 and LTC6993-4 allow the output pulse to be “retriggered”. As shown in Figure 4, the output pulse will stay high until  $t_{OUT}$  after the last rising-edge on TRIG. Successive trigger signals can extend the pulse width indefinitely. Consecutive trigger signals must be separated by  $t_{RETRIG}$  to be recognized.

Negative Trigger Versions

In addition to the retrigger option, the LTC6993 family also includes negative input (falling-edge) versions. These four combinations are detailed in Table 2.

Table 2. Retrigger and Input Polarity Options

DEVICE	INPUT POLARITY	RETRIGGER
LTC6993-1	Rising-Edge	No
LTC6993-2	Rising-Edge	Yes
LTC6993-3	Falling-Edge	No
LTC6993-4	Falling-Edge	Yes

Output Polarity (POL Bit)

Each variety of LTC6993 also offers the ability to invert the output, producing negative pulses. This option is programmed, along with  $N_{DIV}$ , by the choice of DIVCODE. (The previous section describes how to program DIVCODE using the DIV pin).

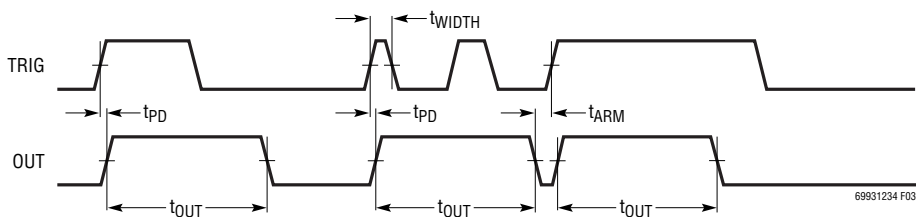


Figure 3. Non-Retriggering Timing Diagram (LTC6993-1, POL = 0)

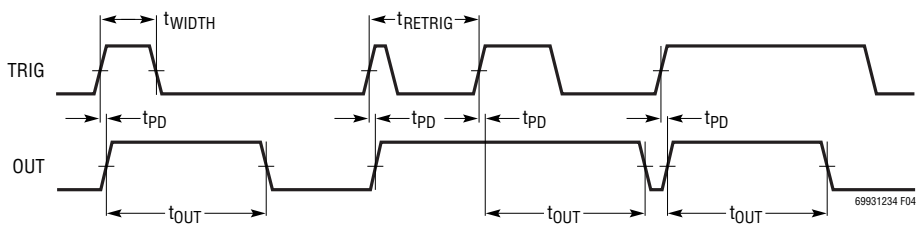


Figure 4. Retriggering Timing Diagram (LTC6993-2, POL = 0)

## OPERATION

### Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring  $V_{DIV}$  for changes. Changes to DIVCODE will be recognized slowly, as the LTC6993 places a priority on eliminating any “wandering” in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \cdot (\Delta DIVCODE + 6) \cdot t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. However, if the output pulse is active during the transition, the pulse width can take on a value between the two settings.

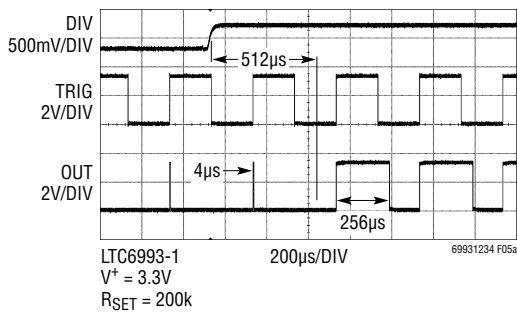


Figure 5a. DIVCODE Change from 0 to 2

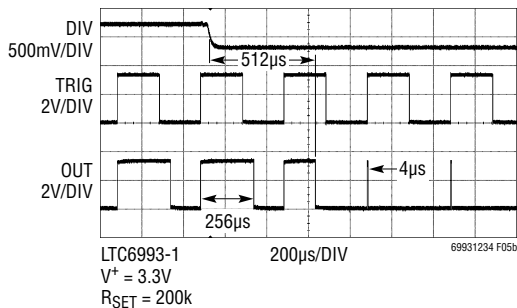


Figure 5b. DIVCODE Change from 2 to 0

### Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time,  $t_{START}$ . The OUT pin is held low during this time. The typical value for  $t_{START}$  ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of  $N_{DIV}$ ):

$$t_{START(TYP)} = 500 \cdot t_{MASTER}$$

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before an output pulse can be generated. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track  $V^+$ . Less than 100pF will not extend the start-up time.

The DIVCODE setting is recognized at the end of the startup up. If  $POL = 1$ , the output will transition high. Otherwise (if  $POL = 0$ ) OUT simply remains low. At this point, the LTC6993 is ready to respond to rising/falling edges on the TRIG input.

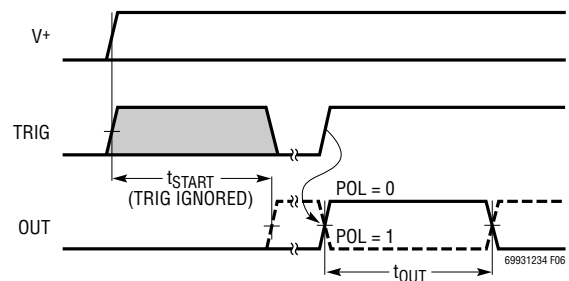


Figure 6. Start-Up Timing Diagram

## APPLICATIONS INFORMATION

### Basic Operation

The simplest and most accurate method to program the LTC6993 is to use a single resistor,  $R_{SET}$ , between the SET and GND pins. The design procedure is a four step process.

#### Step 1: Select the POL Bit Setting.

The LTC6993 can generate positive or negative output pulses, depending on the setting of the POL bit. The POL bit is the DIVCODE MSB, so any DIVCODE  $\geq 8$  has POL = 1 and produces active-low pulses.

#### Step 2: Select LTC6993 Version.

Two input-related choices dictate the proper LTC6993 for a given application:

- Is TRIG a rising or falling-edge input?
- Should retriggering be allowed?

Use Table 2 to select a particular variety of LTC6993.

#### Step 3: Select the $N_{DIV}$ Frequency Divider Value.

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the  $N_{DIV}$  value. For a given output pulse width ( $t_{OUT}$ ),  $N_{DIV}$  should be selected to be within the following range:

$$\frac{t_{OUT}}{16\mu s} \leq N_{DIV} \leq \frac{t_{OUT}}{1\mu s} \quad (1)$$

To minimize supply current, choose the lowest  $N_{DIV}$  value. However, in some cases a higher value for  $N_{DIV}$  will provide better accuracy (see Electrical Characteristics).

Table 1 can also be used to select the appropriate  $N_{DIV}$  values for the desired  $t_{OUT}$ .

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or  $V_{DIV}/V^+$  ratio to apply to the DIV pin.

#### Step 4: Calculate and Select $R_{SET}$ .

The final step is to calculate the correct value for  $R_{SET}$  using the following equation:

$$R_{SET} = \frac{50k}{1\mu s} \cdot \frac{t_{OUT}}{N_{DIV}} \quad (2)$$

Select the standard resistor value closest to the calculated value.

*Example:* Design a one-shot circuit that satisfies the following requirements:

- $t_{OUT} = 100\mu s$
- Negative Output Pulse
- Rising-Edge Trigger Input
- Retriggerable Input
- Minimum power consumption

#### Step 1: Select the POL Bit Setting.

For inverted (negative) output pulse, choose POL = 1.

#### Step 2: Select the LTC6993 Version.

A rising-edge retriggerable input requires the LTC6993-2.

#### Step 3: Select the $N_{DIV}$ Frequency Divider Value.

Choose an  $N_{DIV}$  value that meets the requirements of Equation (1), using  $t_{OUT} = 100\mu s$ :

$$6.25 \leq N_{DIV} \leq 100$$

Potential settings for  $N_{DIV}$  include 8 and 64.  $N_{DIV} = 8$  is the best choice, as it minimizes supply current by using a large  $R_{SET}$  resistor. POL = 1 and  $N_{DIV} = 8$  requires DIVCODE = 14. Using Table 1, choose  $R1 = 102k$  and  $R2 = 976k$  values to program DIVCODE = 14.

#### Step 4: Select $R_{SET}$ .

Calculate the correct value for  $R_{SET}$  using Equation (2):

$$R_{SET} = \frac{50k}{1\mu s} \cdot \frac{100\mu s}{8} = 625k$$



## APPLICATIONS INFORMATION

Since 625k is not available as a standard 1% resistor, substitute 619k if a  $-0.97\%$  shift in  $t_{OUT}$  is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 7.

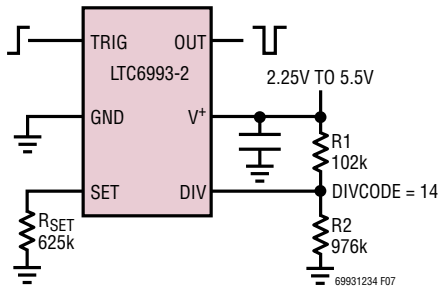


Figure 7. 100µs Negative Pulse Generator

### Voltage-Controlled Pulse Width

With one additional resistor, the LTC6993 output pulse width can be manipulated by an external voltage. As shown in Figure 8, voltage  $V_{CTRL}$  sources/sinks a current through  $R_{MOD}$  to vary the  $I_{SET}$  current, which in turn modulates the pulse width as described in Equation (3).

$$t_{OUT} = \frac{N_{DIV} \cdot R_{MOD}}{50k\Omega} \cdot \frac{1\mu s}{1 + \frac{R_{MOD}}{R_{SET}} - \frac{V_{CTRL}}{V_{SET}}} \quad (3)$$

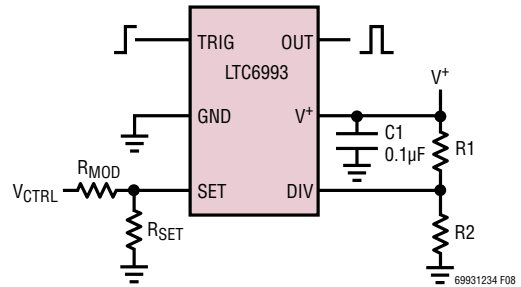


Figure 8. Voltage-Controlled Pulse Width

### Digital Pulse Width Control

The control voltage can be generated by a DAC (digital-to-analog converter), resulting in a digitally-controlled pulse width. Many DACs allow for the use of an external reference. If such a DAC is used to provide the  $V_{CTRL}$  voltage, the  $V_{SET}$  dependency can be eliminated by buffering  $V_{SET}$  and using it as the DAC's reference voltage, as shown in Figure 9. The DAC's output voltage now tracks any  $V_{SET}$  variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC's REF input would affect the pulse width.

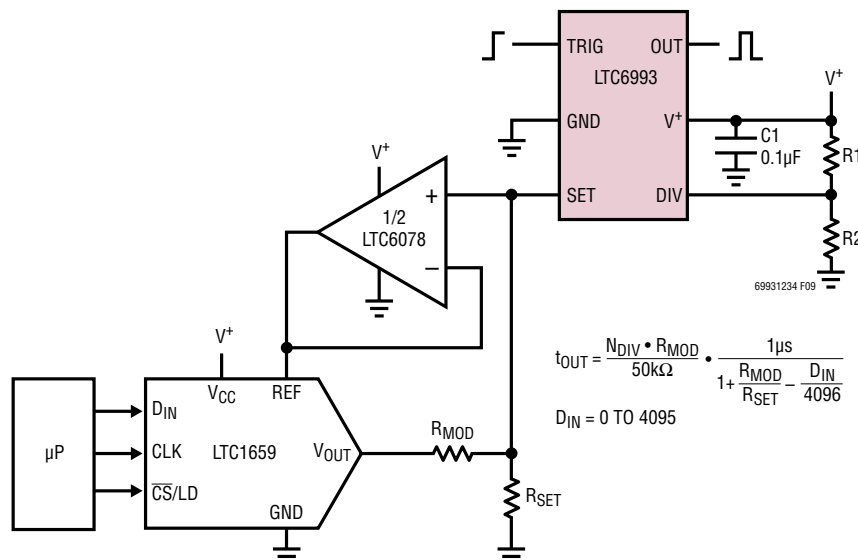


Figure 9. Digitally Controlled Pulse Width

## APPLICATIONS INFORMATION

### $I_{SET}$ Extremes (Master Oscillator Frequency Extremes)

When operating with  $I_{SET}$  outside of the recommended  $1.25\mu A$  to  $20\mu A$  range, the master oscillator operates outside of the  $62.5kHz$  to  $1MHz$  range in which it is most accurate.

The oscillator will still function with reduced accuracy for  $I_{SET} < 1.25\mu A$ . At approximately  $500nA$ , the oscillator will stop. Under this condition, the output pulse can still be initiated, but will not terminate until  $I_{SET}$  increases and the master oscillator starts again.

At the other extreme, it is not recommended to operate the master oscillator beyond  $2MHz$  because the accuracy of the DIV pin ADC will suffer.

### Settling Time

Following a  $2\times$  or  $0.5\times$  step change in  $I_{SET}$ , the output pulse width takes approximately six master clock cycles ( $6 \cdot t_{MASTER}$ ) to settle to within 1% of the final value. An example is shown in Figure 10, using the circuit in Figure 8.

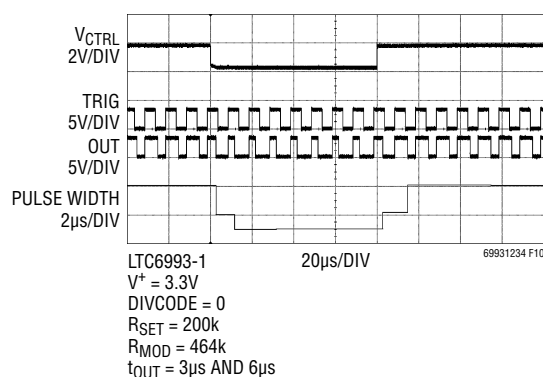


Figure 10. Typical Settling Time

### Coupling Error

The current sourced by the SET pin is used to bias the internal master oscillator. The LTC6993 responds to changes in  $I_{SET}$  almost immediately, which provides excellent settling time. However, this fast response also makes the SET pin sensitive to coupling from digital signals, such as the TRIG input.

Even an excellent layout (examples are provided in the next section) will allow *some* coupling between TRIG and

SET that can affect fast output pulses. Additional error is included in the specified accuracy for  $N_{DIV} = 1$  to account for this.

A very poor layout can actually degrade performance further. The PCB layout should avoid routing SET next to TRIG (or any other fast-edge, wide-swing signal).

### Power Supply Current

The Electrical Characteristics table specifies the supply current while the part is idle (waiting to be triggered).  $I_{S(IDLE)}$  varies with the programmed  $t_{OUT}$  and the supply voltage. Once triggered, the supply current increases while the timing circuit is active:

$$I_{S(ACTIVE)} = I_{S(IDLE)} + \Delta I_{S(ACTIVE)}$$

Using the following equations, the typical supply current can be calculated under any conditions. The increase in current  $\Delta I_{S(ACTIVE)}$  depends on the output loading and the percentage of time that the circuit is active, which can be expressed as a duty cycle. For example, if  $t_{OUT} = 1\mu s$  and the input is triggered every  $2\mu s$ , the output duty cycle will be 50%, which is the same amount of time the LTC6993 is active. Note that these equations account for load capacitance, but ignore resistive loads for simplicity.

If  $N_{DIV} \leq 64$  (DIVCODE = 0-2, 13-15):

$$I_{S(IDLE)} = \frac{V^+}{t_{MASTER}} \cdot 7pF + \frac{V^+}{t_{OUT}} \cdot 4pF + \frac{V^+}{500k\Omega} + 2.2 \cdot I_{SET} + 50\mu A$$

$$\Delta I_{S(ACTIVE)} \cong \text{DutyCycle}$$

$$\cdot \left( \frac{V^+}{t_{MASTER}} \cdot 5pF + \frac{V^+}{t_{OUT}} \cdot (20pF + C_{LOAD}) \right)$$

If  $N_{DIV} \geq 512$  (DIVCODE = 3-12):

$$I_{S(IDLE)} = \frac{V^+}{t_{MASTER}} \cdot 7pF + \frac{V^+}{500k\Omega} + 1.8 \cdot I_{SET} + 50\mu A$$

$$\Delta I_{S(ACTIVE)} \cong \text{DutyCycle} \cdot \frac{V^+}{t_{OUT}} \cdot C_{LOAD}$$

## APPLICATIONS INFORMATION

### Supply Bypassing and PCB Layout Guidelines

The LTC6993 is an accurate monostable multivibrator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 11 shows example PCB layouts for both the SOT-23 and DCB packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6993. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V<sup>+</sup> and GND pins using a low inductance path. The connection from C1 to the V<sup>+</sup> pin is easily done directly on the top layer. For the DCB package, C1's connection to GND is also simply done on the top layer. For the SOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the

C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1μF ceramic capacitor.

2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R<sub>SET</sub> as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the output pulse width. Having a short connection minimizes the exposure to signal pickup.
4. Connect R<sub>SET</sub> directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

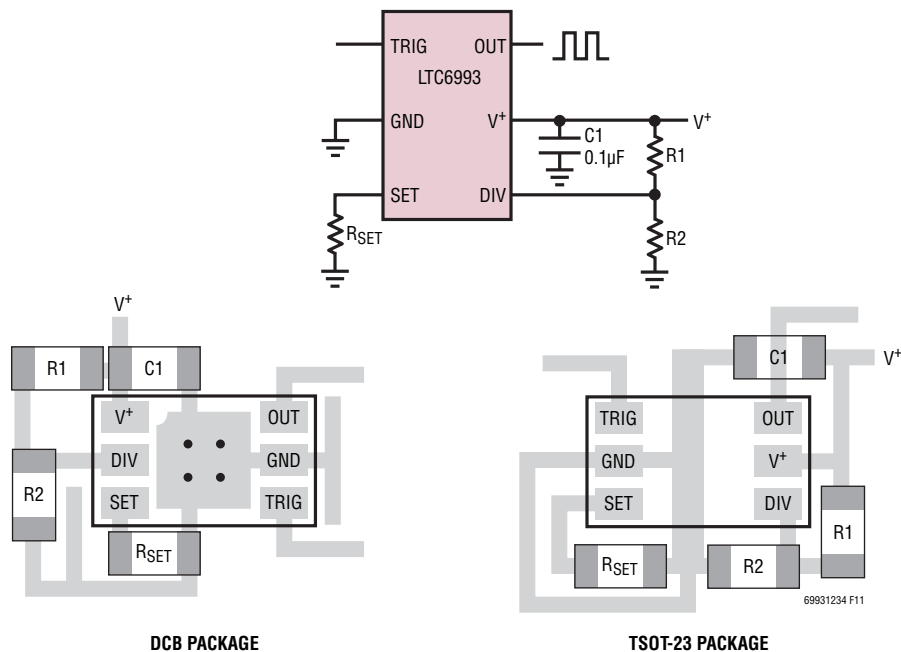
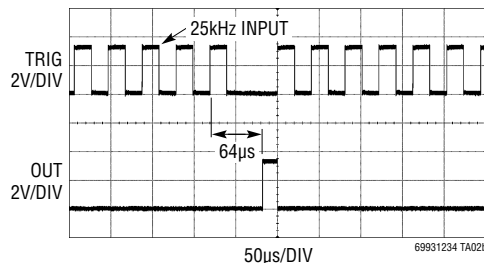
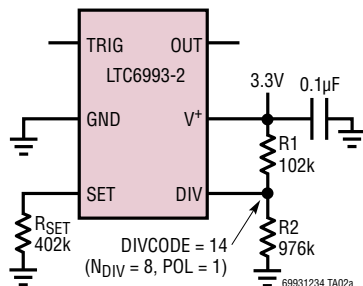


Figure 11. Supply Bypassing and PCB Layout

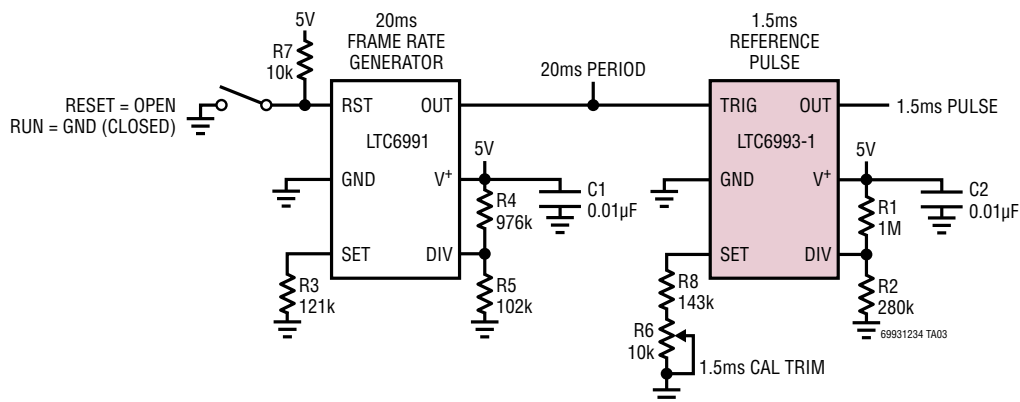
## TYPICAL APPLICATIONS

### Missing Pulse Detector

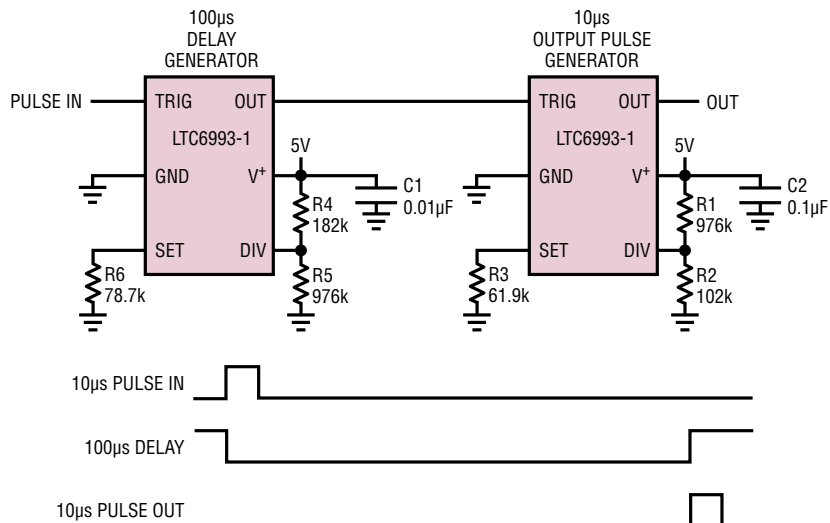


Use retriggerable one shot with output inverted. Output remains low as long as retrigger occurs within t<sub>OUT</sub> = 64μs.

### 1.5ms Radio Control Servo Reference Pulse Generator

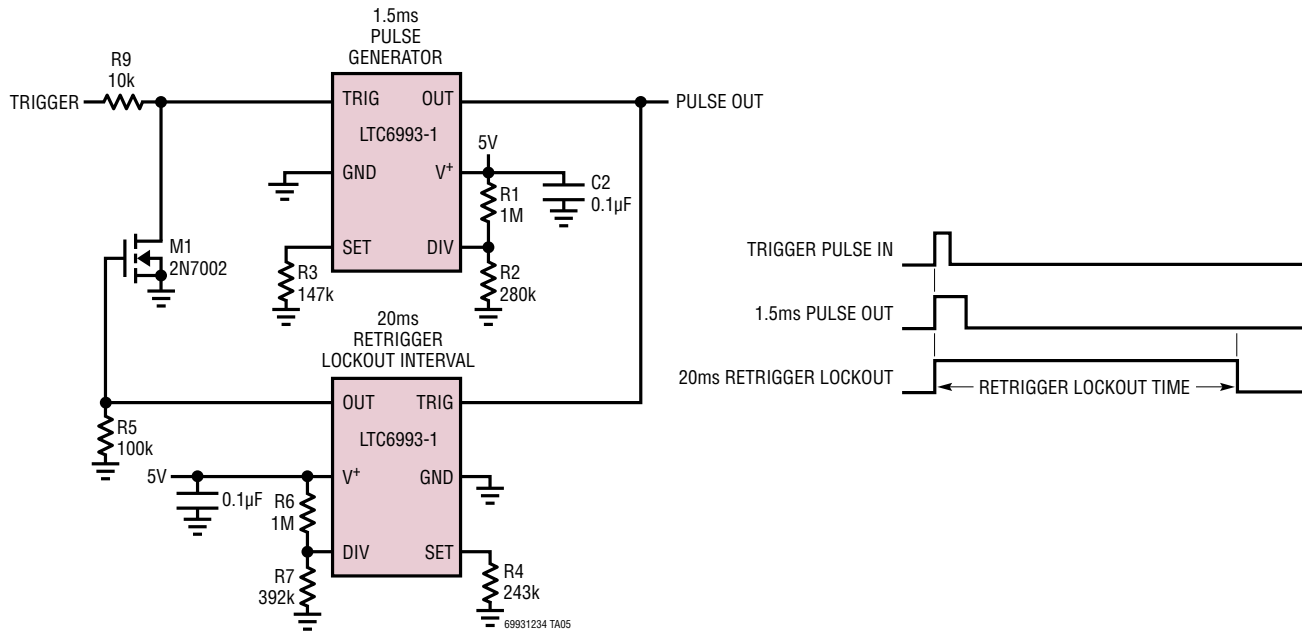


### Pulse Delay Generator

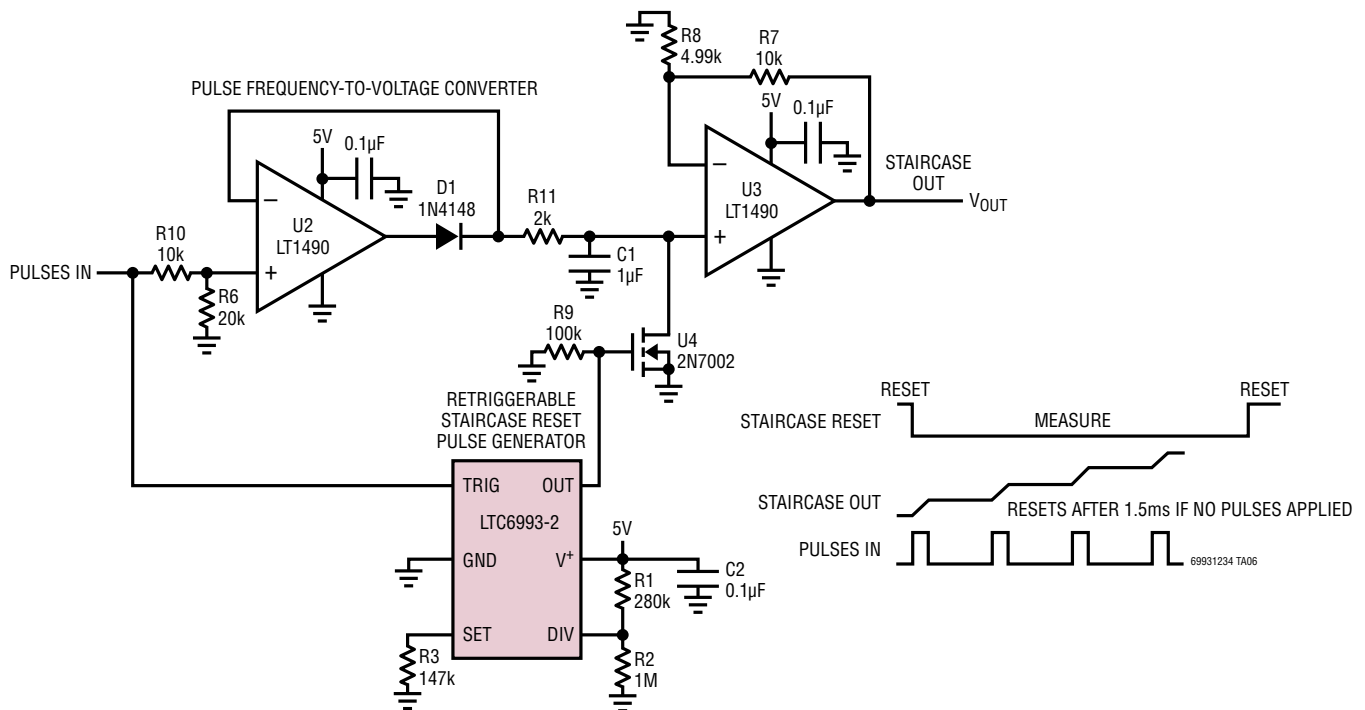


## TYPICAL APPLICATIONS

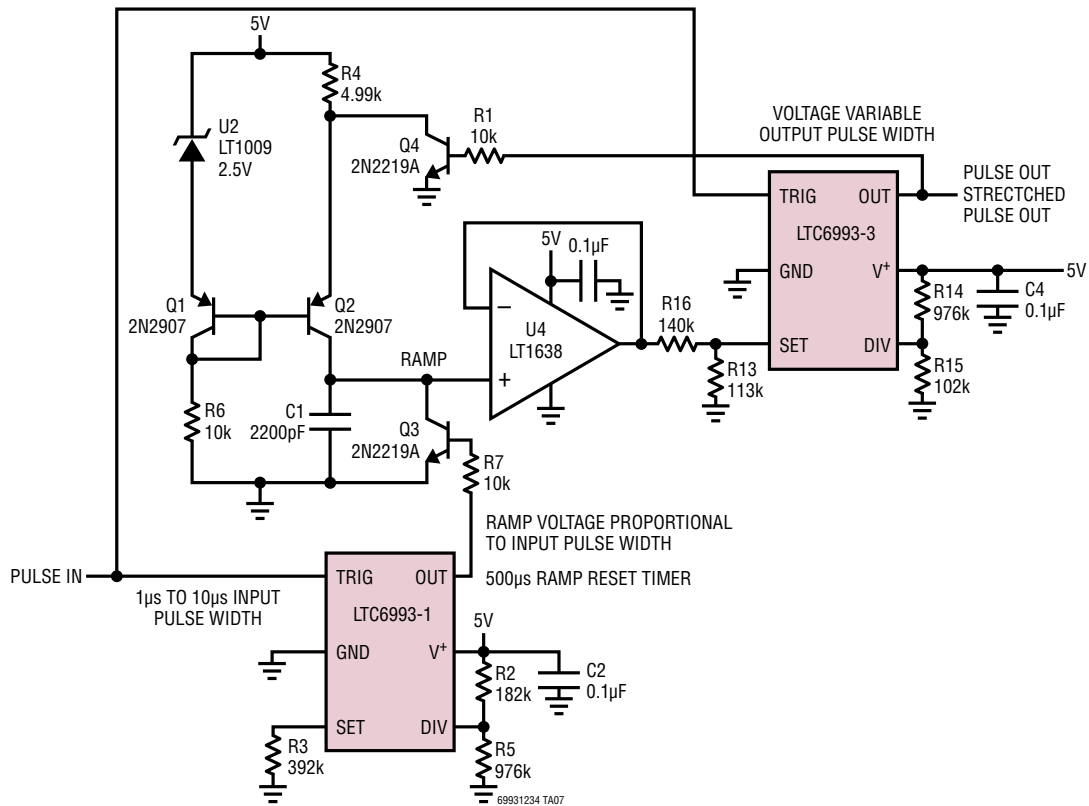
### RC Servo Pulse Generator Controlled Retrigger Lockout Time Interval



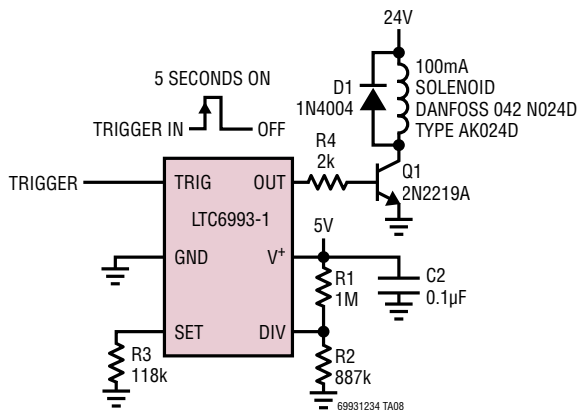
### Pulse Frequency-to-Voltage Converter



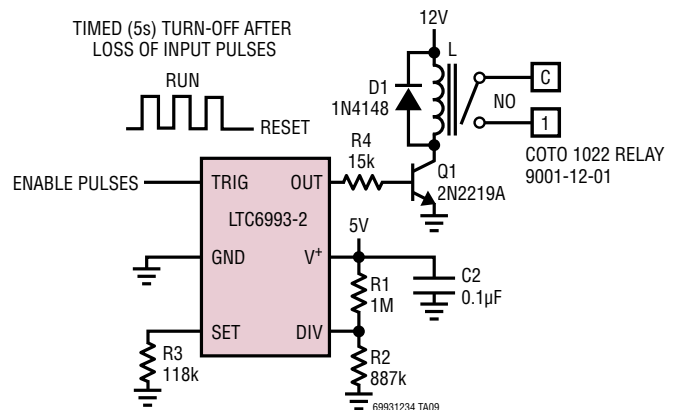
### Pulse Stretcher



### On-Time Programmable Pulsed Solenoid Driver

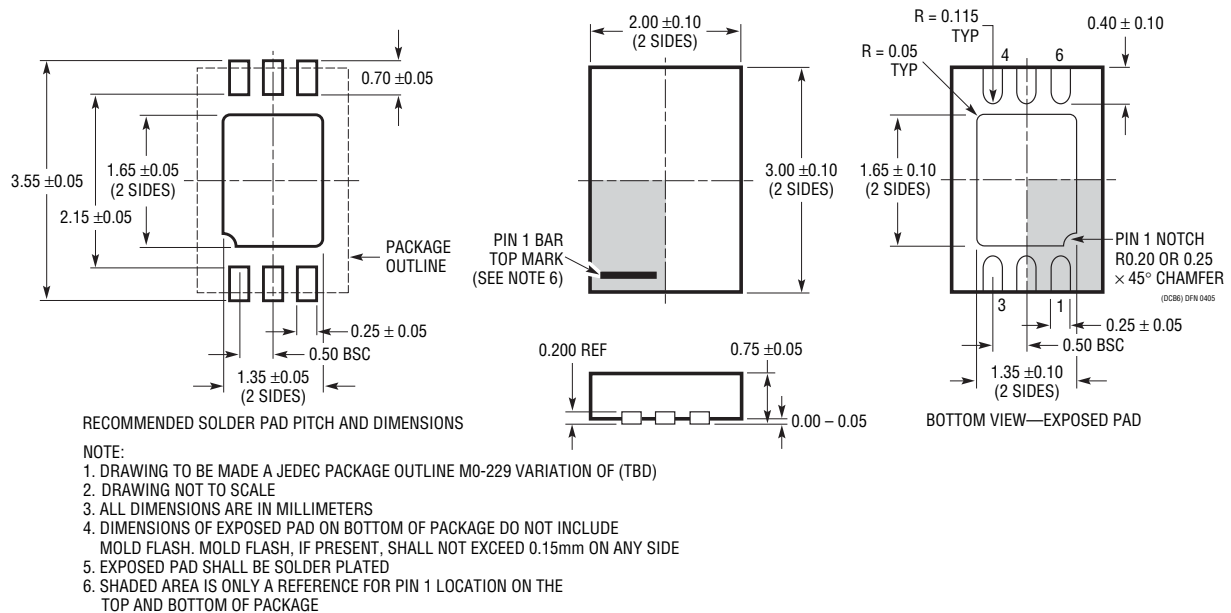


### Safety Time-Out Relay Driver

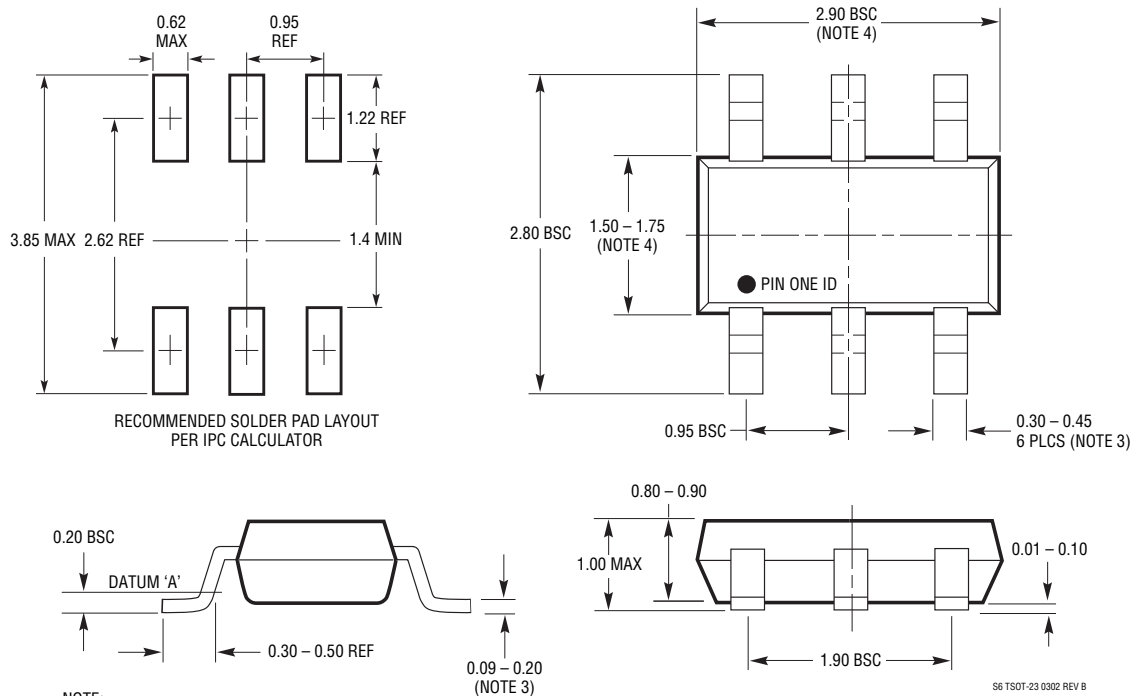


## PACKAGE DESCRIPTION

### DCB Package 6-Lead Plastic DFN (2mm × 3mm) (Reference LTC DWG # 05-08-1715 Rev A)



### S6 Package 6-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1636)



The circuit diagram shows three LTC6993-3 one-shot timers connected in series. The first timer is an LTC6994-1, and the other two are LTC6993-3. Each timer has a TRIG input, an OUT output, and a DIV pin. The TRIG inputs are connected in series, with the first timer's TRIG input connected to a START TEST SEQUENCE signal. The OUT output of each timer is connected to the TRIG input of the next timer. The DIV pins are connected to a common bus labeled "SHARED DIV PIN BIASING FOR EQUAL ONE-SHOT TIMERS". This bus is connected to a 5V supply through a resistor R10 (25k) and a potentiometer R9 (30s DELAY ADJUST). The output of the third timer is connected to a 5V supply through a resistor R5 (1000k) and a potentiometer R4 (681k). The timing diagram shows the START TEST SEQUENCE signal, followed by three sequential test pulses labeled TEST 1, TEST 2, and TEST 3. The pulses are separated by a DELAY period.

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
LTC6900	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
LTC6906/LTC6907	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator	Micropower, I <sub>SUPPLY</sub> = 35µA at 400kHz
LTC6930	Fixed Frequency Oscillator, 32.768kHz to 8.192MHz	0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz
LTC6990	TimerBlox: Voltage-Controlled Silicon Oscillator	Fixed-Frequency or Voltage-Controlled Operation
LTC6991	TimerBlox: Resettable Low Frequency Oscillator	Clock Periods up to 9.5 hours
LTC6992	TimerBlox: Voltage-Controlled Pulse Width Modulator (PWM)	Simple PWM with Wide Frequency Range
LTC6994	TimerBlox: Delay Block/Debouncer	Delay Rising Edge, Falling Edge or Both Edges